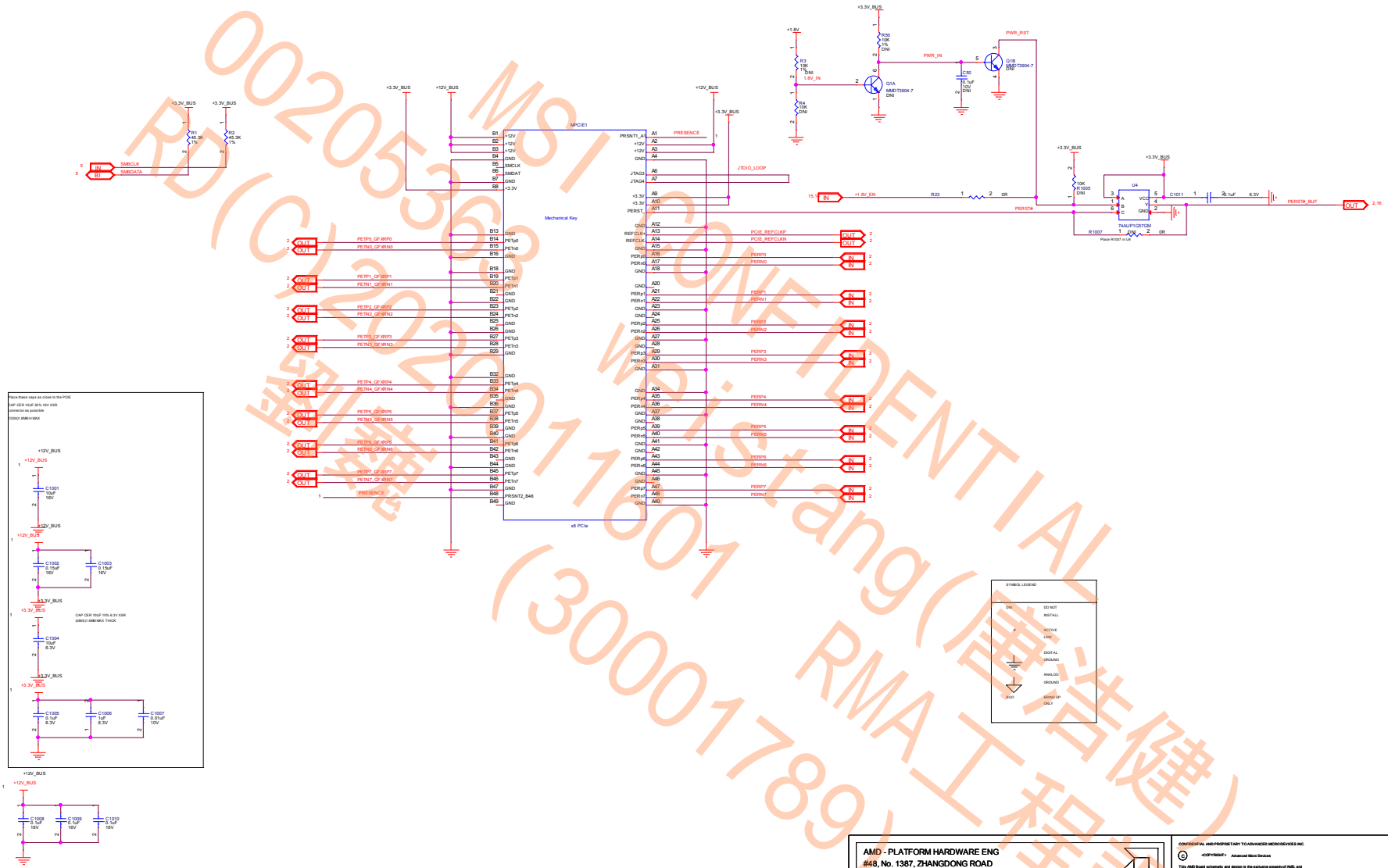


# PCI-EXPRESS EDGE CONNECTOR

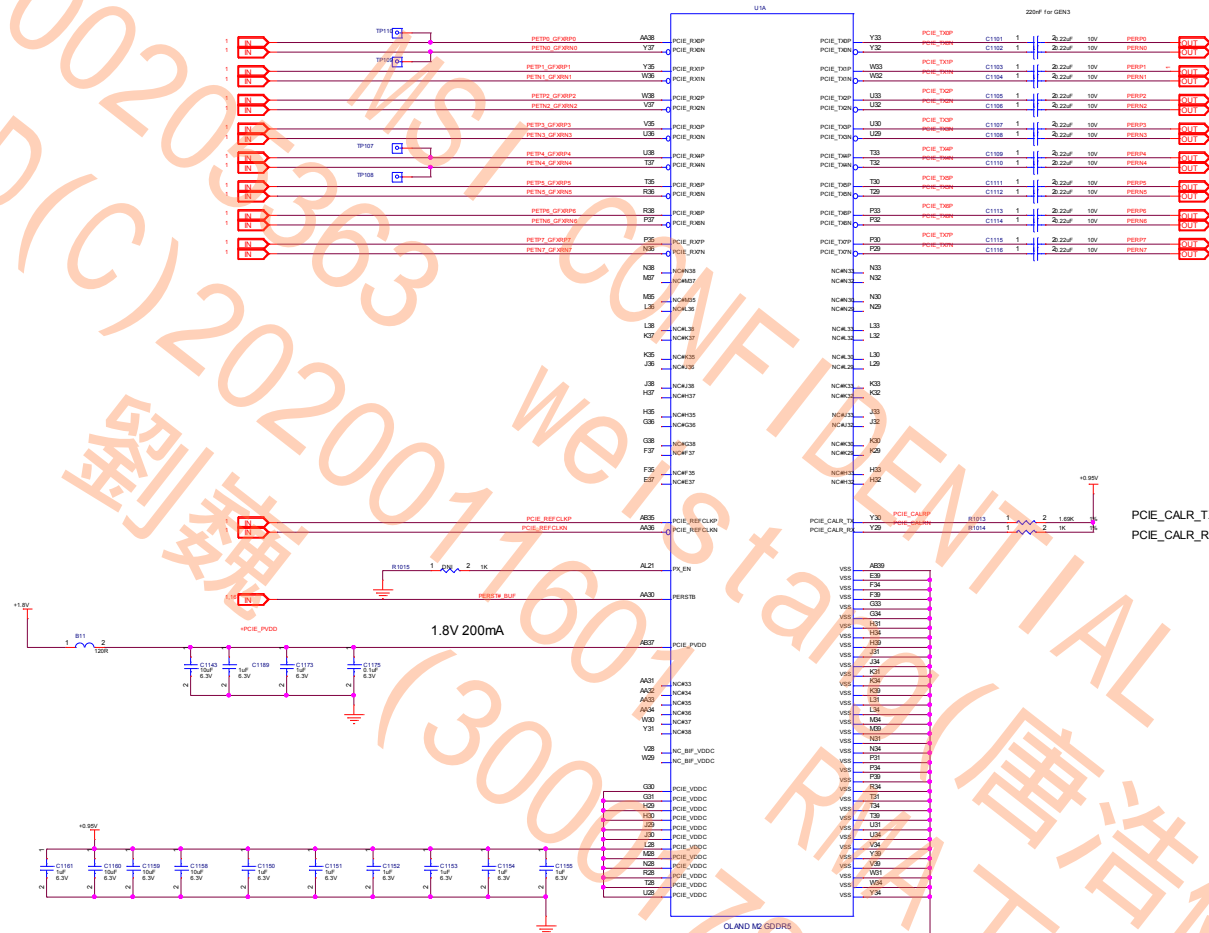


<b>AMD - PLATFORM HARDWARE ENG</b> #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203			
<b>SHEET:</b> PCIe Edge Connector		<b>REV:</b> 2.0	
<b>DATE:</b> Tue Sep 22 06:34:19 2015		<b>SHEET NUMBER:</b> 1 OF 20	
<b>DOCUMENT NUMBER:</b> 105-C869w-008		<b>TITLE:</b> Oland G5 2GB VGA/SDVI/HDMI/DP	

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Oland PCIe Interface

NOTE: Some of the PCIe waypoints will  
be available through vias on traces.

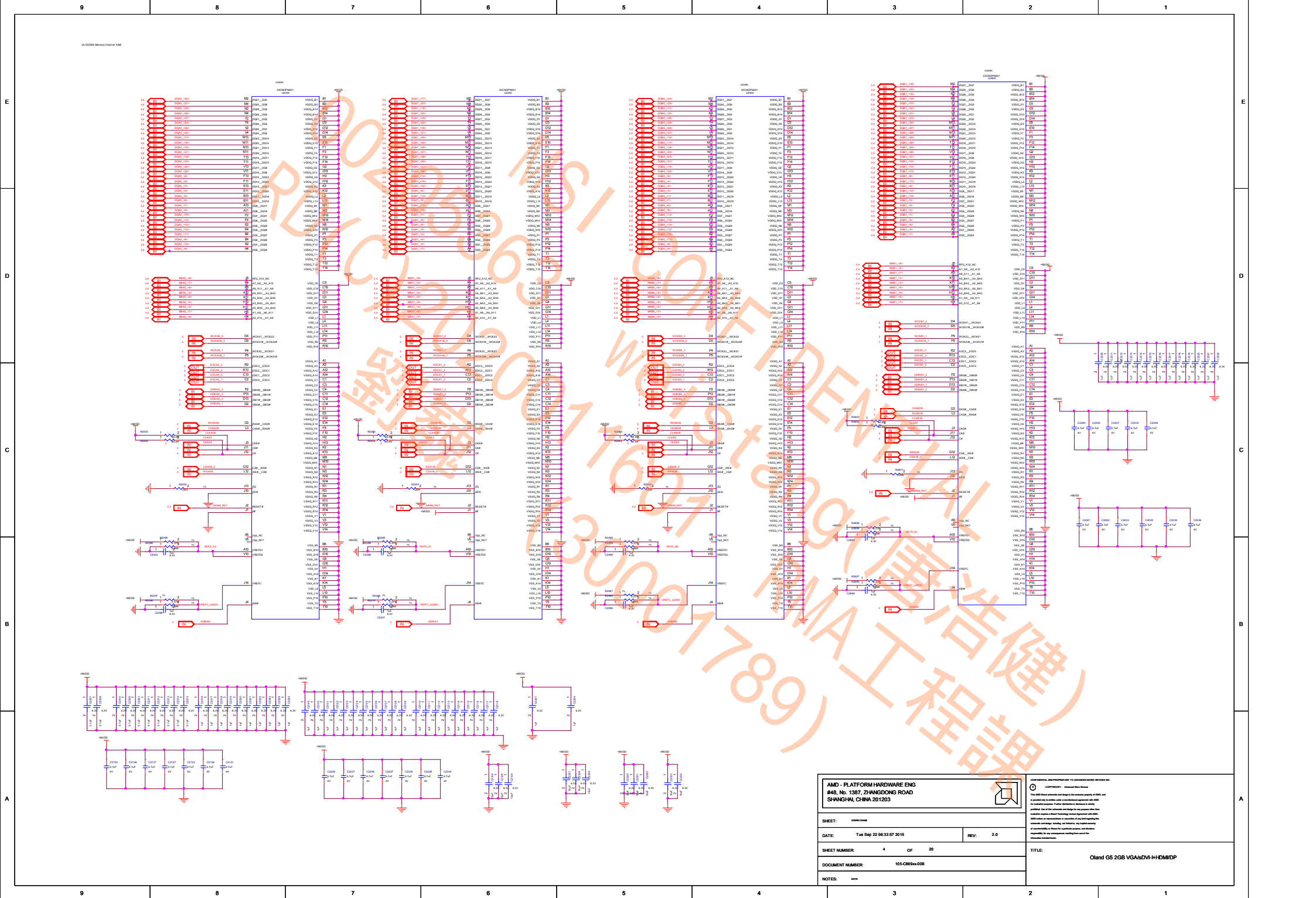


PCIe\_CALR\_TX 1.69k pull up for Oland  
PCIe\_CALR\_RX 1k pull up for Oland

AMD - PLATFORM HARDWARE ENG #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203		
SHEET:	Oland PCIe Interface	
DATE:	Mon Sep 21 10:06:43 2015	REV: 2.0
SHEET NUMBER:	2	OF 20
DOCUMENT NUMBER:	105-C869w-008	

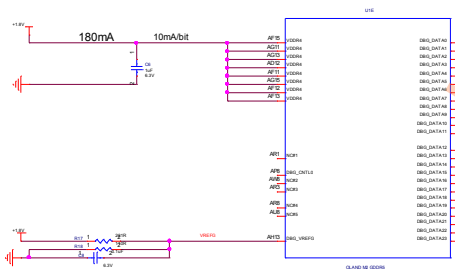
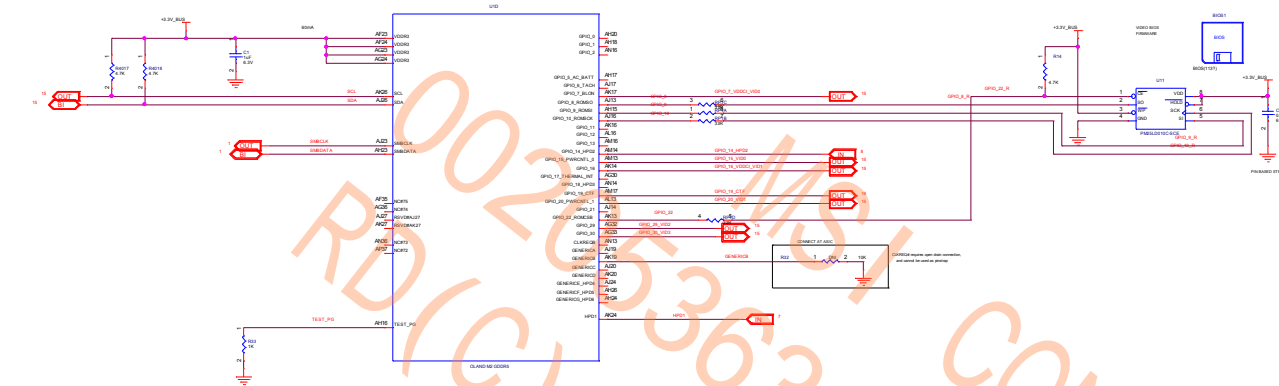
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TITLE: Oland G5 2GB VGA/DVI-HDMI/DP		





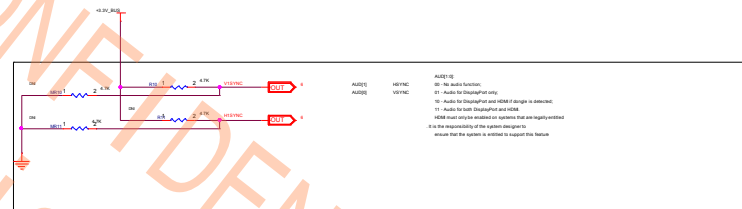
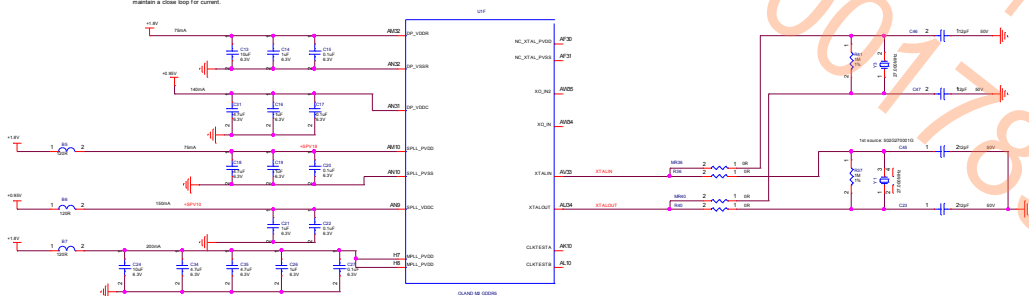
OLAND GPIOs Strap CF XTAL OSC

PN 2280079000 For 108K (PMDLV101A-100SC)



Place the crossfile  
testpoints near the ASIC and  
not the connector

Please pay attention to the grounding  
strategies for these filter capacitors to  
maintain a close loop for current.



AMD - PLATFORM HARDWARE ENG  
#48, No. 1387, ZHANGDONG ROAD  
SHANGHAI, CHINA 201203

SHEET: Oland GPIO Strap P1

DATE: Mon Sep 21 16:05:39 2015

SHEET NUMBER: 5 OF 20

DOCUMENT NUMBER: 105-CH80x-008

NOTES: none



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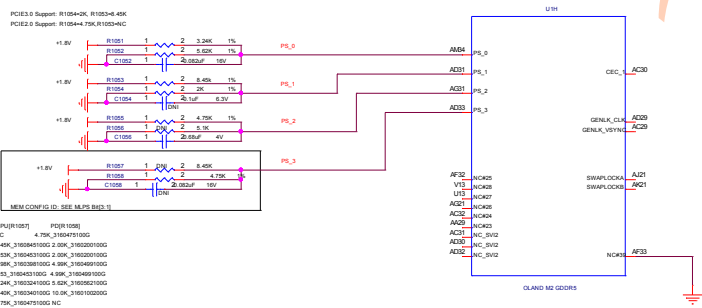
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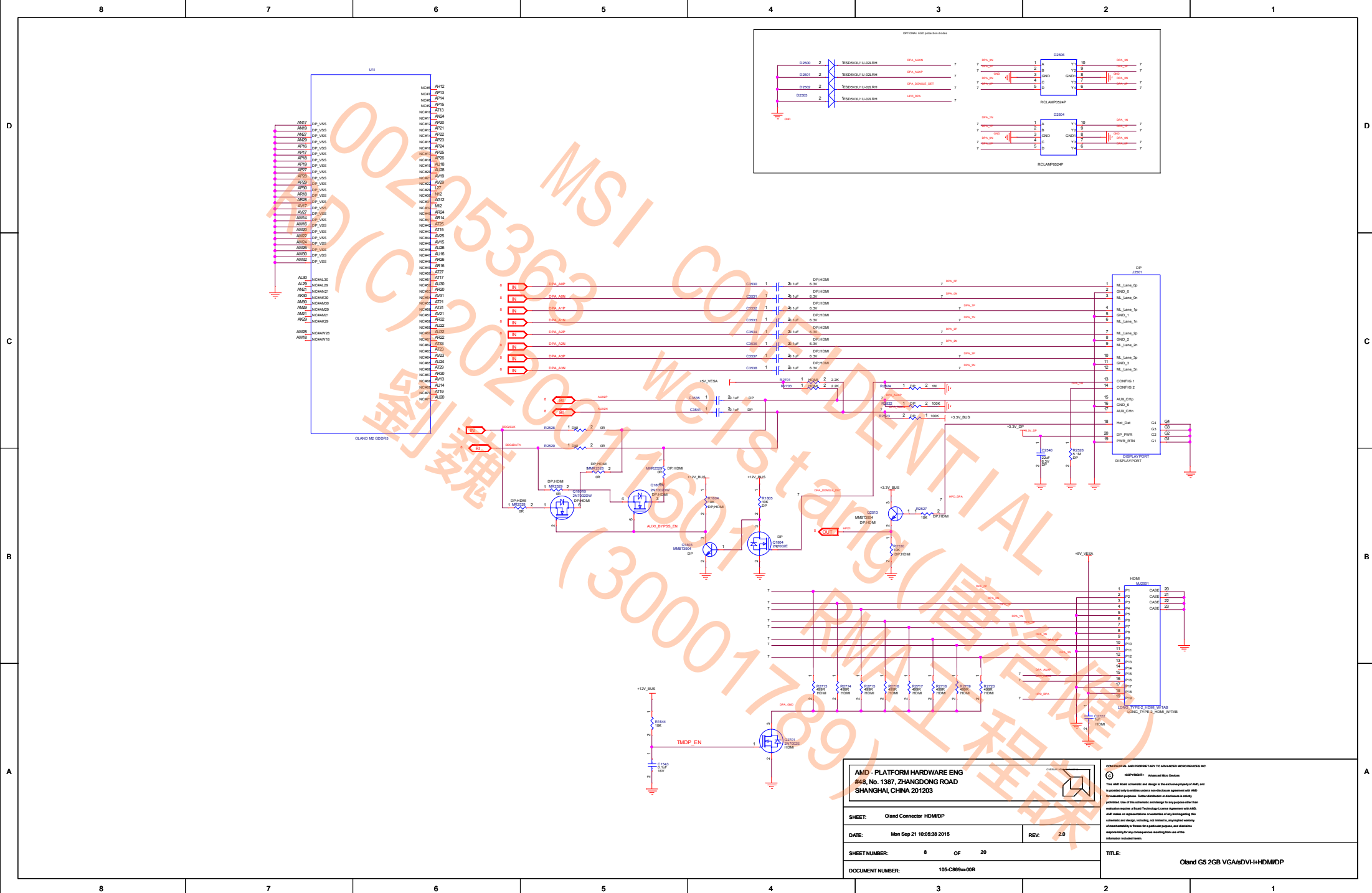
responsibility for any consequences resulting from use of the

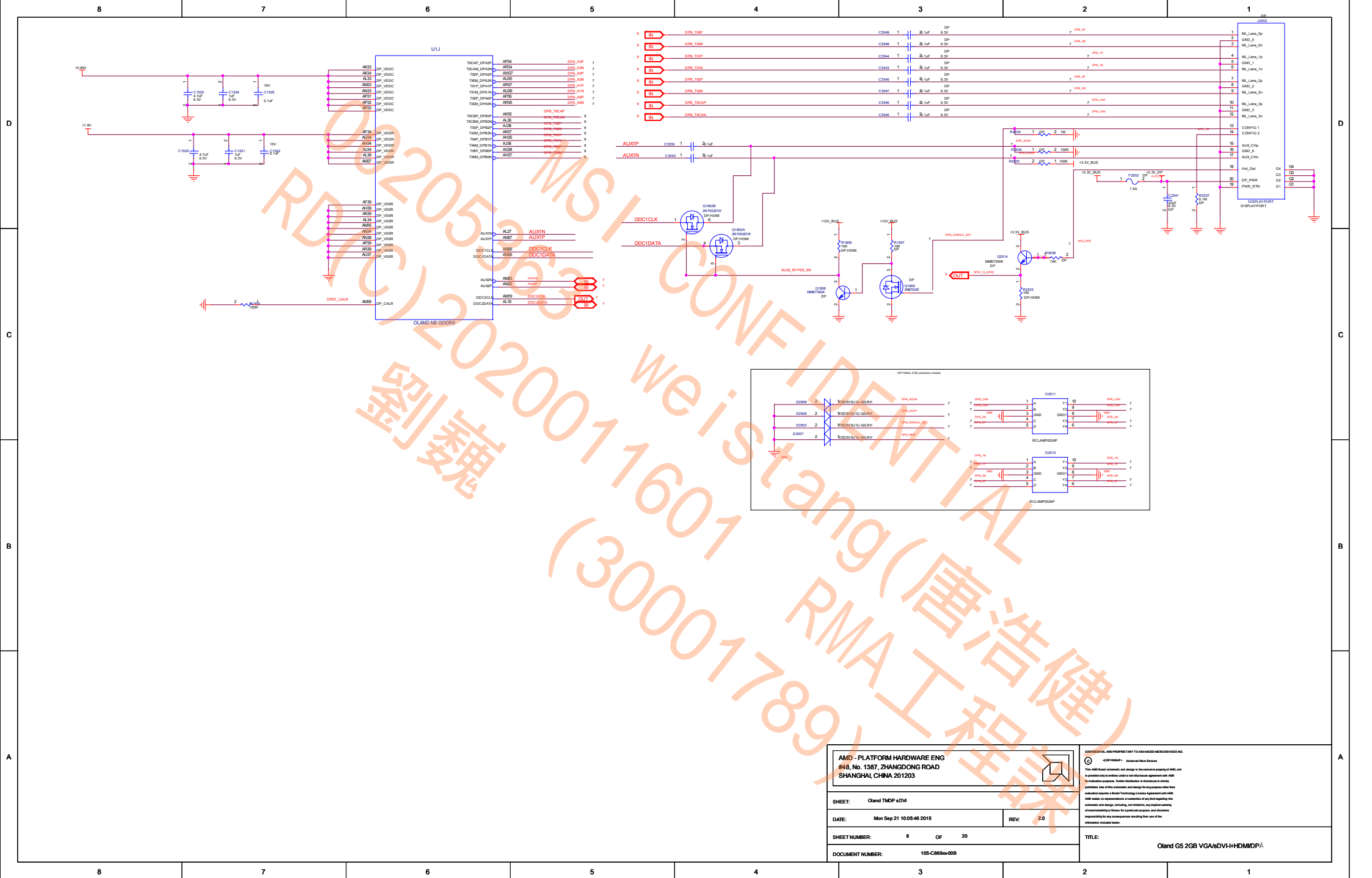
contents and design.

TITLE: Oland G5 2GB VGA/40W/40W/40W/40W



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<p><b>SHEET:</b>      <b>Clad DAC and MLPs</b></p>	<p><b>REV:</b>      <b>2.0</b></p>	
<p><b>DATE:</b>      <b>Tue Sep 22 06:32:58 2015</b></p>	<p><b>TITLE:</b></p> <p style="text-align: center; font-weight: bold;">Clad 5x 2GB VGAs/DVI-I/HDMI/DP</p>	
<p><b>SHEET NUMBER:</b>      <b>6</b>      <b>OF</b>      <b>20</b></p>	<p><b>DOCUMENT NUMBER:</b>      <b>105-C869ex-00B</b></p>	
<p><b>NOTES:</b>      <b>NOTE</b></p>		

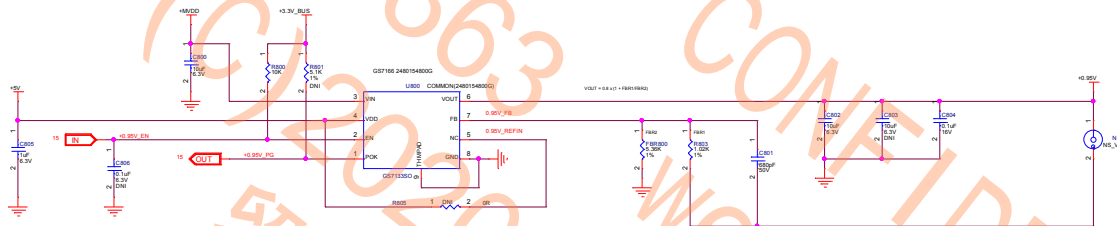






Linear Regulators

Load #1:  $V_{in} = +1.5V \pm 2\%$   $V_{out} = +0.95V \pm 2\%$   $I_{out} = 1.44A$  (TYP) RMS MAX  
PCB: 50 to 70mm sq, copper area for cooling



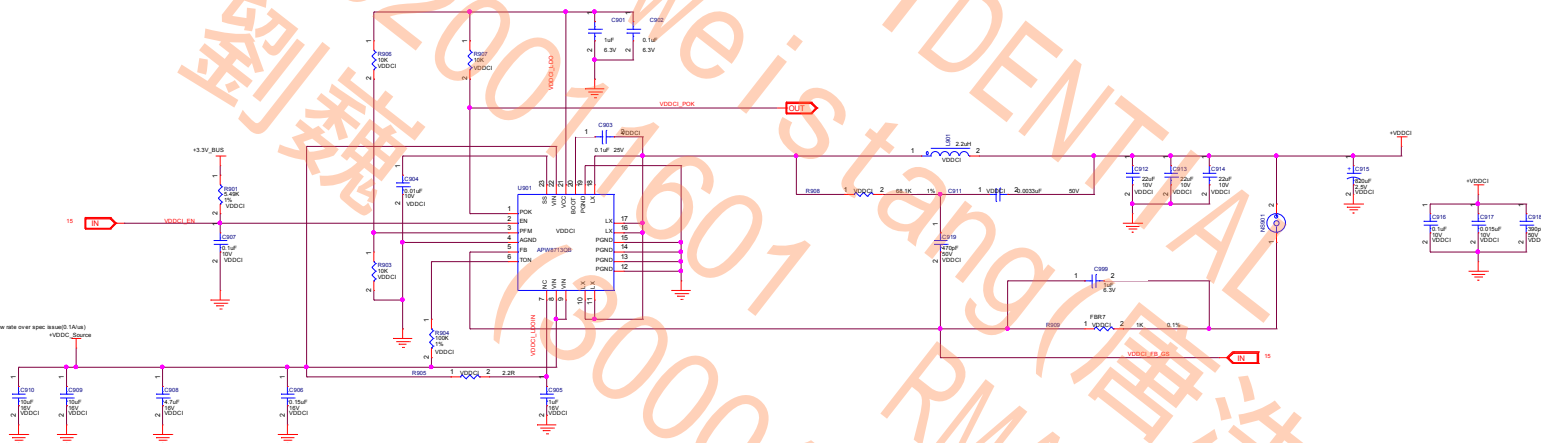
AMD - PLATFORM HARDWARE ENG #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: 0.95V	
DATE: Mon Sep 21 10:06:44 2015	REV: 2.0
SHEET NUMBER: 10 OF 20	TITLE:
DOCUMENT NUMBER: 105-C869-008	

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Oland G5 2GB VGA/4xHDMI/DP	



Regulator for M100

Use rVDDC\_Source to share L801 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)  
rVDDC\_Source



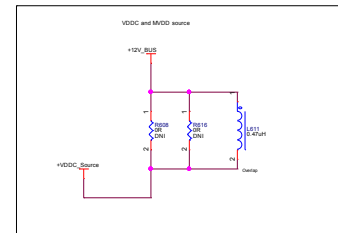
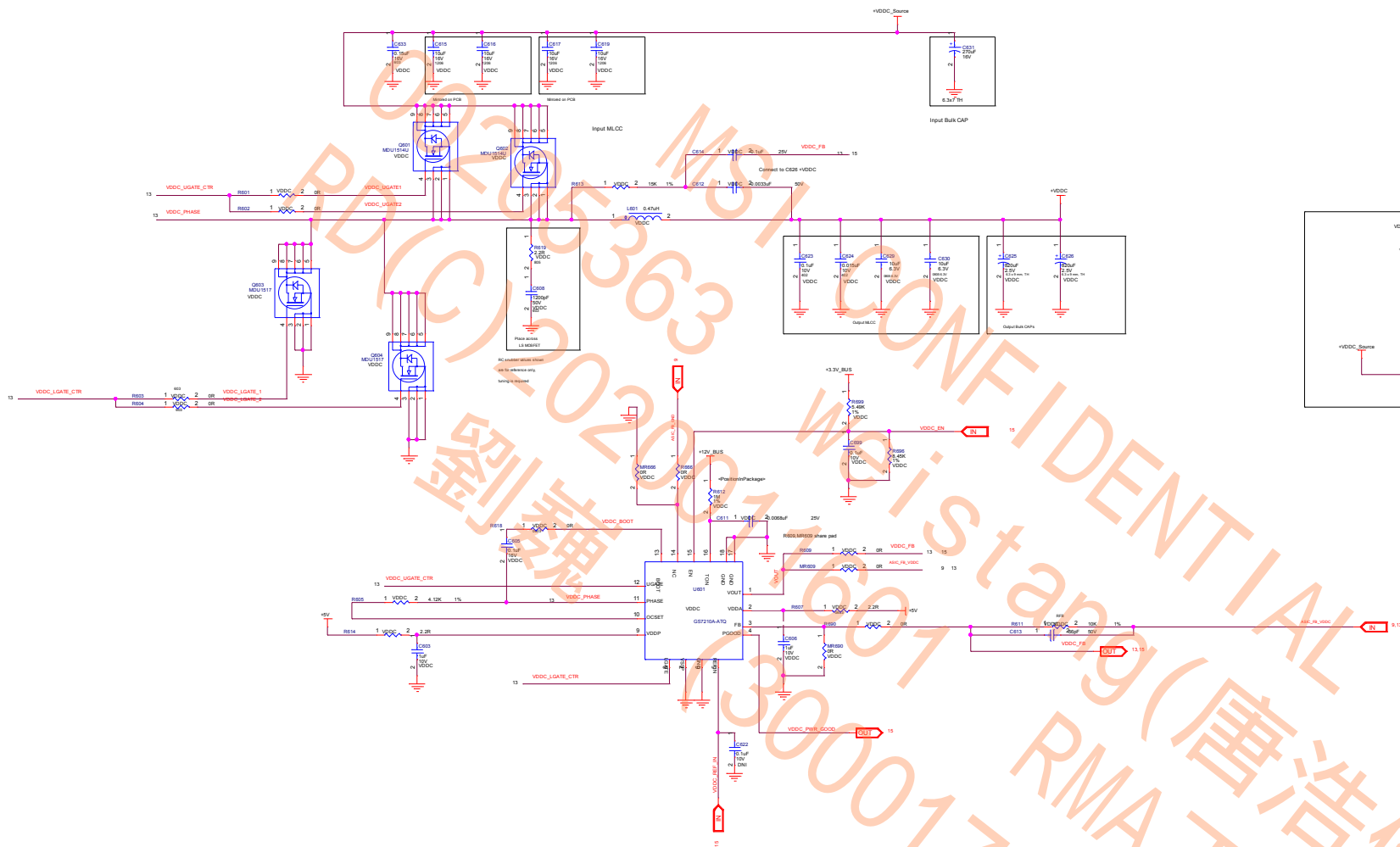
AMD - PLATFORM HARDWARE ENG  
#48, No. 1387, ZHANGDONG ROAD  
SHANGHAI, CHINA 201203



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SHEET:	VDDCI		
DATE:	Tue Sep 22 06:32:59 2015	REV:	2.0
SHEET NUMBER:	12	OF	20
DOCUMENT NUMBER:	105-C869a-008		
NOTES:	NOTE		

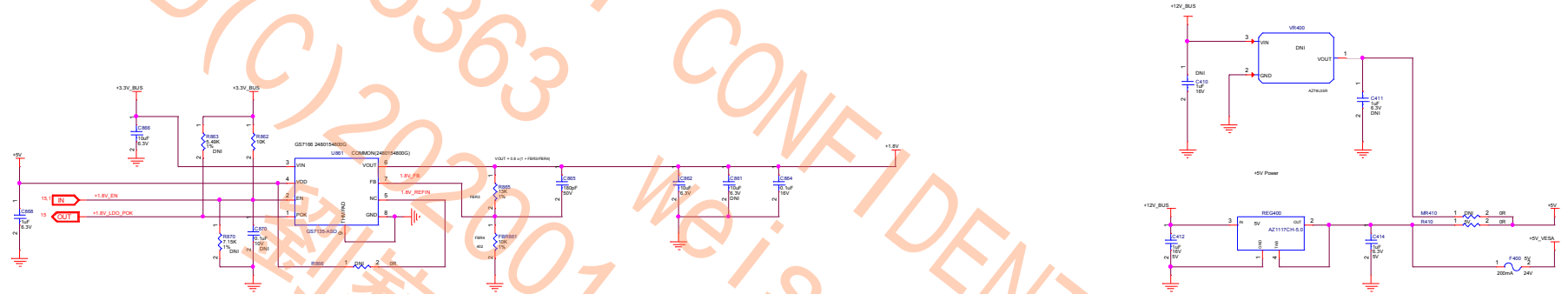
TITLE:  
Oland G5 2GB VGA/sDVI-HDMI/DP




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SHEET: VDDC		REV: 2.0	TITLE:
DATE: Mon Sep 21 10:05:41 2015			Oland G5 2GB VGA+DVI+HDMI+DP
SHEET NUMBER: 13 OF 20			
DOCUMENT NUMBER: 105-C889-008			

Linear Regulators

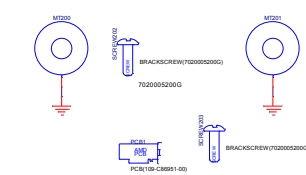
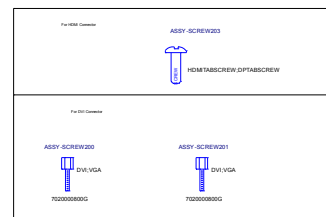
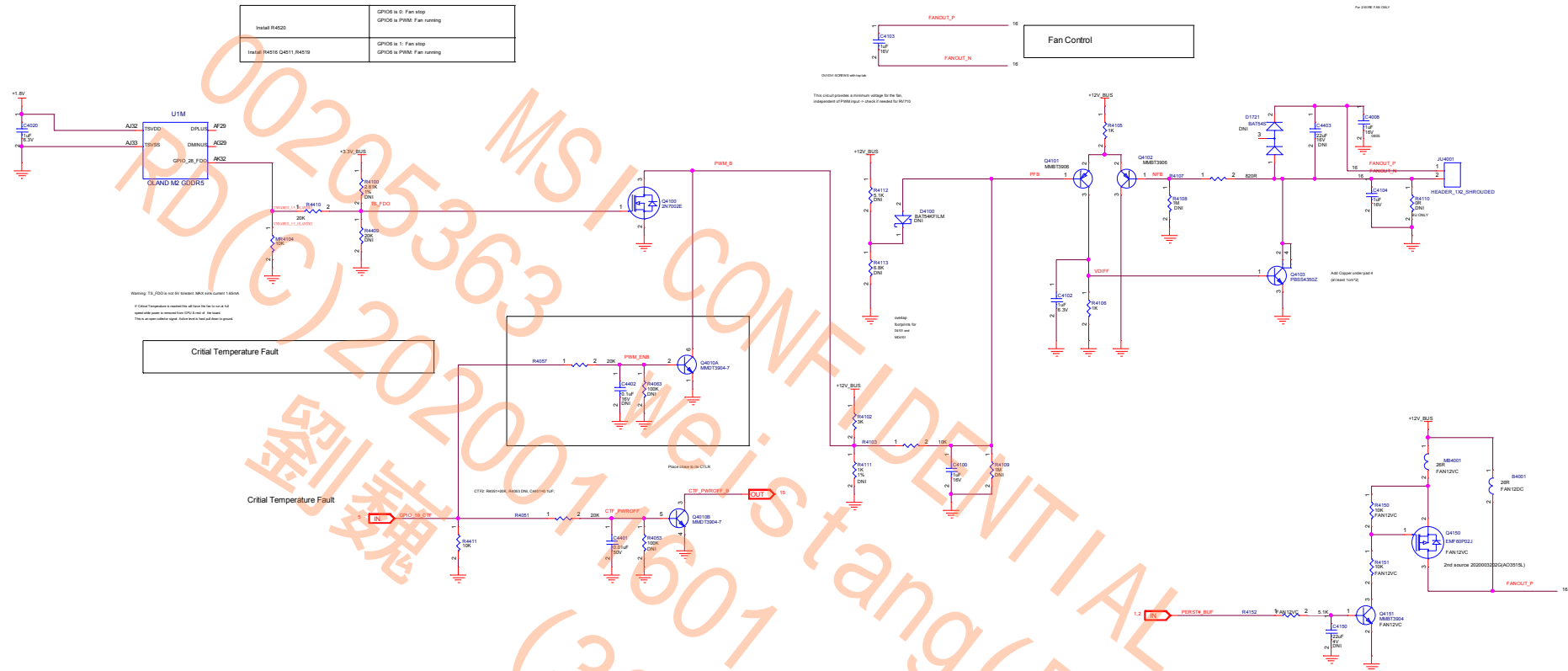
LDO #2:	Vin = 3.00V to 3.60V (3.3V $\pm$ 5%)	Vout = +1.8V $\pm$ 2%	Iout = 1.5A (75V) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			



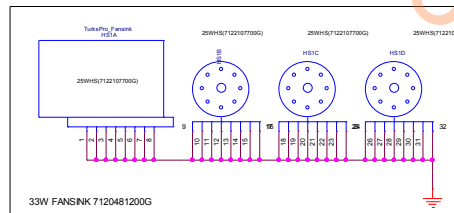
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SHEET:		Linear Regulators		REV:		2.0		TITLE:
DATE:		Mon Sep 21 10:06:44 2015						
SHEET NUMBER:		14 OF 20						
DOCUMENT NUMBER:		105-C869rev-008		Oland G5 2GB VGA+DVI+HDMI DP				




## Mechanical and Thermal Management



Bracket, VGA, HDMI, DVI	8020055200G
Bracket, VGA, DP(tab), DVI	80200552A0G
Bracket, LP, DP(tab), DVI	8020055300G
Bracket, LP, HDMI, DVI	80200553A0G



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<p><b>SHEET:</b>            <b>Med/Thermal Management</b></p>	
<p><b>DATE:</b>            <b>Mon Sep 21 10:05:42 2015</b></p>	<p><b>REV:</b>            <b>2.0</b></p>
<p><b>SHEET NUMBER:</b>            16            OF            20</p>	
<p><b>DOCUMENT NUMBER:</b>            105-C869xx-00B</p>	
<p><b>TITLE:</b></p> <p style="text-align: right;"><b>Oland G5 2GB VGA+eDVI+HDMI+DP</b></p>	



DW-L	HPD4	DDCAUJM
HDIM	HPD1	DDCAUJM
DP	HPD3	DDCAUJM

GPIO5	VDDC_VDD	
GPIO25	VDDC_VDD1	
GPIO7	VDDC_VDD	DEFAULT1
GPIO5	VR_HDT	

12V\_BUS  
5.5A

MVDD SOURCE  
1.5A

1.5V@10A

VDDCI SOURCE  
0.6A

1.05V@6A

VDDC PHASE1 SOURCE  
2.7A

VDDC@25A

VDDC PHASE2 SOURCE  
2.7A

VDDC@25A

FAN  
0.5A

3.3V\_BUS  
3A

0.95V SOURCE  
1A

0.95V@1A

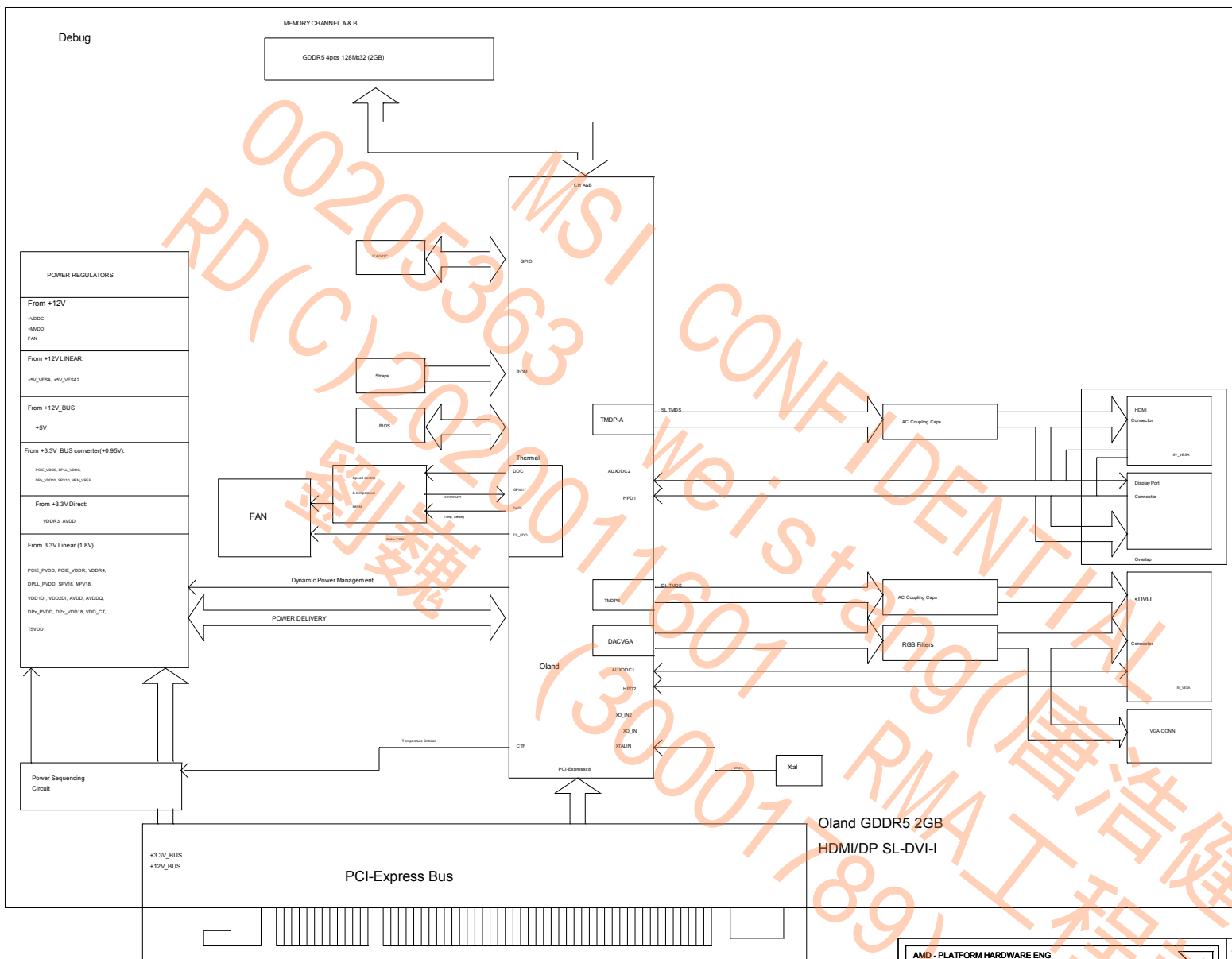
1.8V\_LDO  
0.5A

1.8V@0.5A

3.3V@60mA

AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: GPIO DDC HPD map	
DATE: Tue Sep 22 06:32:59 2015	REV: 2.0
SHEET NUMBER: 18	OF 20
DOCUMENT NUMBER: 105-C8690x-008	
NOTES: NOTE	

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TITLE: Oland G5 2GB VGA/DVI-HDMI/DP



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SHEET: BLOCK DIAGRAM	
DATE: Fri Sep 18 08:34:41 2015	REV: 2.0
SHEET NUMBER: 19 OF 20	
DOCUMENT NUMBER: 105-C869rev-008	

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TITLE: Oland G5 2GB VGA/HDV-I-HDMI-DP	

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AMD



TITLE:

Oland G6 2GB VGA/6DVI+HDMI/DP

DOCUMENT NUMBER:

105-C889wa-008

DATE:

Tue Sep 22 02:20:17 2015

SHEET NUMBER:

20 OF 20

REV:

2.0

REVISION HISTORY

ENGINEER:

Tony Yang

NOTES:

NOTE

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SCH Rev

PCB Rev

Date

REVISION DESCRIPTION

1.00

000

06/19/14

1 Initial release

2.00

000

09/22/15

2 AMD VGA, 4K

8

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